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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,114	YANG, SAM	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,3,5-8,13-25,29,74-78,83,84,90,91,96,102,106,111,113-115,119,121-123 and 127* is/are allowed.

6)☒ Claim(s) *4,9-11,26,30,32,79,80,85,86,92,97,98,103,104,112,116,117,120,124 and 125* is/are rejected.

7)☒ Claim(s) *27,31,82,89,95 and 101* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 2-11,13-27,29-32,74-80,82-86,89-92,95-98,101-104,106,111-117,119-125 and 127.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Shinriki et al.. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has an orthorhombic crystalline structure. It is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30).

Claims 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Shinriki et al.. As to claim 9, Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, and a metal oxide buffer layer (3)(col. 6, lines 54-55) interposed between and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, wherein the buffer layer, embodied as a tantalum oxide layer, includes the refractory metal tantalum.

As to claim 10, Shinriki et al. discloses (col. 6, lines 54-55) that the metal component of the buffer layer is tantalum.

As to claim 11, it is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30).

Claim 26 is rejected under 35 U.S.C. 102(b) as being anticipated by Shinriki et al.. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the metal oxide buffer layer, embodied as a tantalum oxide layer, has an orthorhombic crystalline structure. It is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30).

Claims 30 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Shinriki et al.. As to claim 30, Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has a dielectric constant greater than that of the dielectric layer, embodied as silicon oxide. It is understood in the art that tantalum oxide has a dielectric constant (about 25) greater than silicon oxide (about 4)(see, for example, Time Domain CVD).

As to claim 32, it is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 79 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ino in view of Shinriki et al.. Ino, Figure 1, discloses a semiconductor die comprising an integrated circuit supported by a substrate (1) and having a plurality (col. 1, line 20-21) of integrated circuit devices wherein at least one of the plurality of integrated circuit devices comprises a capacitor (10), (11) and (12). Ino does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and a metal oxide buffer layer interposed between and directly adjoining the dielectric layer and the second electrode, wherein the buffer layer has an orthorhombic crystal lattice structure. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has an orthorhombic crystalline structure. It is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the die of Ino with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Ino to obtain the invention as specified in claim 79.

Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ino in view of Shinriki et al.. Ino, Figure 1, discloses a semiconductor die comprising an integrated circuit supported by a substrate (1) and having a plurality (col. 1, line 20-21) of integrated circuit devices wherein at least one of the plurality of integrated circuit devices comprises a capacitor (10), (11) and (12). Ino does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and a metal oxide buffer layer interposed between and directly adjoining the dielectric layer and the second electrode, wherein the buffer layer has dielectric constant greater than the dielectric layer. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound

dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has a dielectric constant greater than that of the dielectric layer, embodied as silicon oxide. It is understood in the art that tantalum oxide has a dielectric constant greater than silicon oxide (see, for example, Time Domain CVD). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the die of Ino with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Ino to obtain the invention as specified in claim 80.

Claim 85 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Shinriki et al.. Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhombic crystalline structure. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has an orthorhombic crystalline structure. It is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Shinriki et al.. The motivation for doing so would have been extend the

lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Yoneda to obtain the invention as specified in claim 85.

Claim 86 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Shinriki et al.. Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has a dielectric constant greater than that of the dielectric layer, embodied as silicon oxide. It is understood in the art that tantalum oxide has a dielectric constant greater than silicon oxide (see, for example, Time Domain CVD). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Yoneda to obtain the invention as specified in claim 86.

Claim 92 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al. in view of Shinriki et al.. Chu et al., Figure 2, discloses a memory module comprising a support (10), a plurality of leads extending from the support (8), a command link (19) coupled to at least one of the plurality of leads, a plurality of data links (Fig. 3, element 54) wherein each data link is coupled to at least one of the plurality of leads and memories (20), (22), (40) and (42) contained on the support and coupled to the

command link, wherein the memories comprise an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Chu et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhombic crystalline structure. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has an orthorhombic crystalline structure. It is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Chu et al. with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Chu et al. to obtain the invention as specified in claim 92.

Claim 97 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Shinriki et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric

layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhombic crystalline structure. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has an orthorhombic crystalline structure. It is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Le et al. with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Le et al. to obtain the invention as specified in claim 97.

Claim 98 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Shinriki et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide

layer, has a dielectric constant greater than that of the dielectric layer, embodied as silicon oxide. It is understood in the art that tantalum oxide has a dielectric constant greater than silicon oxide (see, for example, Time Domain CVD). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Le et al. with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Le et al. to obtain the invention as specified in claim 98.

Claim 103 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Shinriki et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein the metal oxide buffer layer has an orthorhombic crystalline structure. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has an orthorhombic crystalline structure. It is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Le et al. with the capacitor of Shinriki et

al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Le et al. to obtain the invention as specified in claim 103.

Claim 104 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Shinriki et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein the metal oxide buffer layer has a dielectric constant greater than the dielectric constant of the dielectric layer. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has a dielectric constant greater than that of the dielectric layer, embodied as silicon oxide. It is understood in the art that tantalum oxide has a dielectric constant greater than silicon oxide (see, for example, Time Domain CVD). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory module of Le et al. with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Le et al. to obtain the invention as specified in claim 104.

Claim 112 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Shinriki et al.. Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda further discloses in Figure 1, a memory cell comprising a capacitor (5) and an access device (1b), embodied as a wordline. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer intermediate and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein the buffer layer has an orthorhombic crystalline structure. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has an orthorhombic crystalline structure. It is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Le et al. to obtain the invention as specified in claim 112.

Claims 116 and 117 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Shinriki et al.. As to claim 116, Yoneda, Figure 4, discloses a memory device comprising an array of memory cells (51) wherein at least one memory cell has a capacitor (Fig. 7, element 5), a row access circuit (53) coupled to the array of memory cells, a column access circuit (54) coupled to the array of memory cells, and an address decoder circuit (52) coupled to the row access circuit and the column access circuit. Yoneda further discloses in Figure 1, a memory cell comprising a capacitor (5) and an

access device (1b), embodied as a wordline. Yoneda does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer intermediate and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein the buffer layer includes a refractory metal. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, and a metal oxide buffer layer (3)(col. 6, lines 54-55) interposed between and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, wherein the buffer layer, embodied as a tantalum oxide layer, includes the refractory metal tantalum. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory device of Yoneda with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Le et al. to obtain the invention as specified in claim 116.

As to claim 117, Shinriki et al. discloses (col. 6, lines 54-55) that the metal component of the buffer layer is tantalum.

Claim 120 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Shinriki et al.. Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. further discloses that the processor is electrically connected to a memory cell via the data link. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide

buffer layer intermediate and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein the buffer layer has an orthorhombic crystalline structure. Shinriki et al., Figure 7, discloses a capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, a metal oxide buffer layer (3)(col. 6, lines 54-55) intermediate and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, and wherein the buffer layer, embodied as a tantalum oxide layer, has an orthorhombic crystalline structure. It is understood in the art that tantalum oxide may be formed with an orthorhombic crystalline structure (see, for example, Doeff et al., col. 5, lines 18-30). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the processor and memory cell of Le et al. with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Le et al. to obtain the invention as specified in claim 120.

Claims 124 and 125 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. in view of Shinriki et al.. As to claim 124, Le et al., Figure 1, discloses a memory system comprising a controller (102), a command link (112) coupled to the controller, a data link (114) coupled to the controller and a memory device (104) coupled to the command link and the data link wherein the memory comprises an array of memory cells with capacitors, a row access circuit coupled to the array of memory cells, a column access circuit coupled to the array of memory cells and an address decoder circuit coupled to the row access circuit and the column access circuit. Le et al. further discloses an electronic system comprising a processor (103) and a circuit module having a plurality of leads (105) coupled to the processor. Le et al. further discloses that the processor is electrically connected to a memory cell via the data link. Le et al. does not disclose expressly the capacitor comprising: a first electrode; a second electrode; a single compound dielectric layer interposed between the first electrode and the second electrode; and at least one metal oxide buffer layer intermediate and directly adjoining the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein the buffer layer has an orthorhombic crystalline structure. Shinriki et al., Figure 7, discloses a

capacitor comprising a first electrode (10)(col. 6, lines 44-46), a second electrode (4), a single compound dielectric layer (2) and (3), interposed between the first electrode and the second electrode, and a metal oxide buffer layer (3)(col. 6, lines 54-55) interposed between and directly adjoining the dielectric layer (2)(col. 6, line 55) and the second electrode, wherein the buffer layer, embodied as a tantalum oxide layer, includes the refractory metal tantalum. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the processor and memory cell of Le et al. with the capacitor of Shinriki et al.. The motivation for doing so would have been to extend the lifetime of the capacitor (Shinriki et al., Abstract). Therefore, it would have been obvious to combine Shinriki et al. with Le et al. to obtain the invention as specified in claim 124.

As to claim 125, Shinriki et al. discloses (col. 6, lines 54-55) that the metal component of the buffer layer is tantalum.

Allowable Subject Matter

Claims 27, 31, 82, 89, 95 and 101 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2, 3, 5-8, 13-25, 29, 74-78, 83, 84, 90, 91, 96, 102, 106, 111, 113-115, 119, 121-123 and 127 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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srw
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